CLAIMS:

1. A packaged chip comprising:

(a) a chip having front and rear surfaces and contacts on said front surface;

(b) a chip carrier attached to said chip, said chip carrier including a dielectric layer extending across one surface of said chip and having an inner surface facing upwardly and an outer surface facing downwardly, said chip carrier having conductive traces thereon electrically connected to said contacts and conductive bumps formed integrally with said traces, said conductive bumps projecting downwardly from said traces, said bumps having bottom ends exposed at the outer surface of said dielectric layer for bonding to contact pads on a circuit panel.

2. A packaged chip as claimed in claim 1 wherein at least one of said bumps has a first wall portion extending downwardly from one of said traces, a bottom wall portion joining said first wall portion adjacent the bottom end of the bump, and a second wall portion extending upwardly from said bottom wall portion to said dielectric layer.

3. A packaged chip as claimed in claim 1 wherein at least one of said bumps is generally U-shaped, with a closed end of the U-shape defining the bottom end of the bump and an open end of the U-shape facing upwardly.

4. A packaged chip as claimed in claim 1 wherein at least one of said bumps is generally cup-shaped, with a closed end of the cup shape defining the bottom end of the bump and an open end of the cup shape facing upwardly.

5. A packaged chip as claimed in claim 1 wherein at least one said generally cup-shaped bump has an imperforate side wall extending upwardly from the bottom end of the bump to said dielectric layer.

6. A packaged chip as claimed in claim 1 wherein at least one of said bumps is substantially solid.

7. A packaged chip as claimed in claim 1 wherein at least one of said bumps has an exterior surface in the form of a surface of revolution about a vertical axis.

8. A packaged chip as claimed in claim 1 wherein at least one of said bumps has a lead-in surface sloping upwardly and outwardly around the entire periphery of the bump adjacent the bottom end of the bump.

9. A packaged chip as claimed in claim 1 wherein at least some of said bumps are disposed in one or more rows at a pitch of 1 mm or less.

10. A packaged chip as claimed in claim 1 wherein said dielectric layer extends beneath said chip, and said inner surface of said dielectric layer faces upwardly toward said chip.

11. A packaged chip as claimed in claim 10 wherein at least some of said bumps are disposed beneath said chip.

12. A packaged chip as claimed in claim 11 wherein all of said bumps are disposed beneath said chip.

13. A packaged chip as claimed in claim 1 wherein said traces are disposed above the outer side of said dielectric layer and said bumps extend at least partially through said dielectric layer.

14. A packaged chip as claimed in claim 13 wherein said traces are disposed on the inner side of said dielectric layer and said bumps extend at least partially through said dielectric layer.

15. A packaged chip as claimed in claim 1 wherein said traces are disposed on the outer side of said dielectric layer.

16. A packaged chip as claimed in claim 10 wherein said front surface of said chip faces downwardly towards said chip carrier.

17. A packaged chip as claimed in claim 16 wherein said chip carrier has leads formed integrally with said traces, said leads being bonded to said contacts of said chip.

18. A packaged chip as claimed in claim 16 further comprising downwardly-facing bonding pads on said chip carrier electrically connected to said traces and bond wires connecting said bonding pads to said contacts.

19. A packaged chip as claimed in claim 18 wherein said bond wires do not extend below the bottom ends of said bumps.

20. A packaged chip as claimed in claim 10 wherein said rear surface of said chip faces downwardly towards said chip carrier.

21. A packaged chip as claimed in claim 20 further comprising upwardly-facing bonding pads on said chip carrier electrically connected to said traces and bond wires connecting said bonding pads to said contacts.

22. A packaged chip as claimed in claim 1 wherein the bottom ends of said conductive bumps are movable with respect to said chip.

23. A packaged chip as claimed in claim 22 wherein the bottom ends of said conductive bumps are movable in a vertical direction towards or away from said chip.

24. A packaged chip as claimed in claim 23 wherein the bottom ends of said conductive bumps are movable in horizontal directions parallel to said surfaces of said chip.

25. A packaged chip as claimed in claim 1 further comprising a spacer layer disposed between said chip and said dielectric layer.

26. A packaged chip as claimed in claim 23 wherein said spacer layer is compliant.

27. A packaged chip as claimed in claim 1 wherein said chip is disposed beneath said dielectric layer and said bumps project downwardly from said dielectric layer beyond said chip.

28. A packaged chip as claimed in claim 25 wherein said front surface of said chip faces toward said outer surface of said dielectric layer.

29. A packaged chip as claimed in claim 1 wherein said bottom ends of said bumps are disposed below said outer surface of said chip carrier.

30. A packaged chip as claimed in claim as claimed in claim 1 wherein said dielectric layer has bump openings therein and said bumps project downwardly from said traces within said bump openings, said bottom ends of said bumps being disposed within said bump openings above said outer surface of said dielectric layer.

31. A coherent, self-supporting chip carrier comprising:

(a) a dielectric layer having an inner surface facing upwardly and an outer surface facing downwardly,

(b) conductive traces on said dielectric layer ;and

(c) conductive bumps formed integrally with said traces, said conductive bumps projecting downwardly from said traces, said bumps having bottom ends adapted for bonding to contact pads on a circuit panel.

32. A chip carrier as claimed in claim 31 wherein at least one of said bumps has a first wall portion extending downwardly from one of said traces, a bottom wall portion joining said first wall portion adjacent the bottom end of the bump, and a second wall portion extending upwardly from said bottom wall portion to said dielectric layer.

33. A chip carrier as claimed in claim 31 wherein at least one of said bumps is generally U-shaped, with a closed end of the U-shape defining the bottom end of the bump and an open end of the U-shape facing upwardly.

34. A chip carrier as claimed in claim 31 wherein at least one of said bumps is generally cup-shaped, with a closed end of the cup shape defining the bottom end of the bump and an open end of the cup shape facing upwardly.

35. A chip carrier as claimed in claim 34 wherein at least one said generally cup-shaped bump has an imperforate side wall extending upwardly from the bottom end of the bump to said dielectric layer.

36. A chip carrier as claimed in claim 34 wherein at the open top end of least one said cup-shaped bump is exposed at the inner surface of said dielectric layer.

37. A chip carrier as claimed in claim 31 wherein at least one of said bumps is substantially solid.

38. A chip carrier as claimed in claim 31 wherein at least one of said bumps has an exterior surface in the form of a surface of revolution about a vertical axis.

39. A chip carrier as claimed in claim 31 wherein at least one of said bumps has a lead-in surface sloping upwardly and outwardly around the entire periphery of the bump adjacent the bottom end of the bump.

40. A chip carrier as claimed in claim 31 wherein at least some of said bumps are disposed in one or more rows at a pitch of 1 mm or less.

41. A chip carrier as claimed in claim 31 wherein said traces are disposed above the outer side of said dielectric layer and said bumps extend at least partially through said dielectric layer.

42. A chip carrier as claimed in claim 41 wherein said traces are disposed on the inner side of said dielectric layer and said bumps extend at least partially through said dielectric layer.

43. A chip carrier as claimed in claim 42 wherein said bumps extend entirely through said dielectric layer and the bottom ends of the bumps are disposed below the outer surface of the dielectric layer.

44. A chip carrier as claimed in claim 31 wherein said traces are disposed on the outer side of said dielectric layer.

45. A chip carrier as claimed in claim 44 wherein said bumps include hollow cup-shaped bumps having open top ends and said dielectric layer extends across the open top ends of at least some of said bumps.

46. A chip carrier as claimed in claim 45 wherein hollow bumps define interior spaces and said dielectric layer extends into the interior spaces of at least some of said bumps.

47. A microelectronic assembly comprising:

(a) a packaged semiconductor chip including:

(i) a chip having front and rear surfaces and contacts on said front surface;

(ii) a chip carrier including a dielectric layer having traces thereon electrically connected to said contacts and bumps integral with said traces, said dielectric layer having an inner surface facing upwardly toward said chip and an outer surface facing downwardly away from said chip, said bumps projecting downwardly from said traces and having bottom ends;

(b) a circuit panel having a top surface and contact pads exposed at said top surface, said bottom ends of said bumps on said chip carrier being bonded to said contact pads on said circuit panel.

48. An assembly as claimed in claim 47 wherein the bottom surface of said chip carrier is spaced vertically from said contact pads by said bumps.

49. An assembly as claimed in claim 47 further comprising an electrically conductive bonding material securing said bumps to said contact pads.

50. An assembly as claimed in claim 49 wherein said conductive bonding material has a minimum thickness less than 50 μm.

51. An assembly as claimed in claim 50 wherein at least some of said bumps define vertically-extensive wall surfaces extending upwardly from the bottom ends of the bumps and said

bonding material forms fillets extending from said contact pads to locations on said wall surfaces above the bottom ends of the bumps defining said wall surfaces.

52. An assembly as claimed in claim 51 wherein said wall surfaces and said fillets extend entirely around at least some of said bumps.

53. An assembly as claimed in claim 52 wherein the bottom ends of said bumps are convex and define a bottom extremity surface merging smoothly with said wall surfaces, and wherein said contact pads are substantially flat.

54. A method of making a microelectronic assembly comprising the steps of:

(a) temporarily engaging a chip assembly including a chip, a chip carrier including a dielectric layer having traces thereon electrically connected to contacts on the chip and bumps integral with the traces with a test fixture so that bottom ends of the bumps projecting downwardly from the traces and projecting downwardly beyond the dielectric layer engage test contacts on the fixture;

(b) testing the chip assembly by transmitting signals between at least some of the engaged bumps and test contacts;

(c) disengaging the chip assembly from the test fixture; and

(d) mounting the tested chip assembly on a circuit panel by bonding the bottom ends of the bumps to contact pads on the circuit panel.

55. A method as claimed in claim 54 wherein, during said step of temporarily engaging, the bottom ends of at least some of said bumps are displaced vertically relative to the bottom ends of others of said bumps.

56. A method as claimed in claim 55 wherein, during said step of temporarily engaging, at least some of said bumps are deformed.

57. A method of making a chip carrier comprising the steps of:

(a) uniting a metal with a dielectric layer having inner and outer surfaces;

(b) forming traces on said dielectric layer from said metal; and

(c) forming metallic bumps by deforming said metal; said uniting, bump-forming and trace-forming steps being performed so that said bumps are integral with said traces and project downwardly from said traces.

58. A method as claimed in claim 57 wherein said bump-forming step is performed after said uniting step.

59. A method as claimed in claim 58 wherein said dielectric layer has openings therein and said bump-forming step is performed so as to deform the metal through at least some of said openings.

60. A method as claimed in claim 59 wherein said deforming step is performed after said trace-forming step.

61. A method as claimed in claim 58 wherein said bump-forming step includes engaging the metal with a tool having projections and moving the tool downwardly relative to the metal so as to form the metal around said projections.

62. A method as claimed in claim 58 wherein said bump-forming step includes engaging said dielectric layer and said metal with a tool and moving said tool so as to deform both said dielectric layer and said metal.

63. A method as claimed in claim 62 wherein said dielectric layer has inner and outer surfaces and said uniting step is performed so as to provide said metal remote from said inner surface of said dielectric layer, the method further comprising providing a spacer layer on said inner surface of said dielectric layer prior to said bump-forming step, said spacer layer being deformed during said bump-forming step.

64. A method as claimed in claim 63 wherein said spacer layer includes an adhesive.

65. A method as claimed in claim 58 wherein said metal is initially in the form of a layer of metal of substantially uniform thickness and wherein said trace-forming step includes deforming the metal to form relatively thick regions and relatively thin regions during the step of deforming the metal to form said bumps, and subsequently removing said relatively thin regions to leave metal in said relatively thick regions as said traces.

66. A socket comprising:

(a) a dielectric layer;

(b) a plurality of unitary, hollow metallic bumps having at least partially closed bottom ends and open top ends mounted on said dielectric layer; and

(c) a substrate having a top surface and contact pads exposed at said top surface, the bottom ends of said bumps being bonded to said contact pads so that said bumps support said dielectric layer above said substrate, the top ends of said bumps being adapted to receive terminals of a microelectronic element to be tested.

67. A socket as claimed in claim 66 wherein said hollow bumps are generally cup-shaped.

68. A socket comprising:

(a) a substrate;

(b) a dielectric layer having thereon test contacts, traces and bumps formed integrally with said traces, said bumps projecting downwardly from said traces and said dielectric layer, said bumps having bottom ends disposed below said dielectric layer, said bumps being interspersed with said test contacts so that said test contacts are offset in horizontal directions from said bumps; and

(c) a substrate having contact pads thereon, said bumps being bonded to said contact pads and supporting said

dielectric layer above said substrate, whereby when terminals of a device to be tested are engaged with said test contacts, said test contacts can be displaced downwardly by flexure of said dielectric layer.